ABSTRACT:

Unified Modeling of Hysteresis and Bias Temperature Instability in WS_2 based FETs

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Field-effect-transistors (FETs) employing two-dimensional transition metal dichalcogenides (2D TMDs) as the channel material have been attracting more and more attention as a promising candidate for the beyond-Moore era of nanoelectronics. Unfortunately, reliability issues plaguing these devices degrade their performance and shorten their lifetime, thereby hampering broad application of these devices for future logic nodes. As such, accurate and predictive modelling of corresponding degradation mechanisms based on a comprehensive physical picture underlying them is of great importance. Most detrimental among these reliability concerns are the hysteresis of current-voltage characteristics featured already by pristine devices and bias temperature instability (BTI). We present an approach to physics-based modelling of the transfer characteristics hysteresis and BTI, which is validated against an extensive set of experimental data acquired using 300-mm-wafer-integrated dual-gated FETs with a tungsten disulphide (WS2) n-type channel and a top gate stack comprised of ALD grown alumina (a-Al2O3) and hafnia (a-HfO2) layers. With the conducted simulations, we show that these two degradation phenomena originate from the same traps present in the gate oxide layer, namely oxygen vacancy (OV) and interstitial aluminium (Ali) in a-Al2O3 and oxygen vacancies and electron (bi-)polarons in a-HfO2. The result of this study is that the hysteresis and BTI are controlled by the mutual energy alignment of the defect band in the dielectric layer and the conduction/valence band of the semiconductor material. Therefore, by means of gate stack engineering to reach a favourable misalignment between these bands one can drastically improve reliability of FETs based on 2D TMDs.